Amendments to the Specification

Please insert the following paragraph before the paragraph beginning on line 7 of page 6:

In addition, the bridging chip **100** includes an input/output interface (IO_INT) **140** coupled to the SIE **125**. The input/output interface **140** is coupled to a memory **142**, a RAM control circuit (RAMCTL) **144** and a global control circuit **146**. The global control circuit **146** is coupled to a translate circuit (XLATE) **148**. The disk interface **115** is coupled to the RAM control circuit **144**, the global control circuit **146**, and the translate circuit **148**.

Please replace the paragraph beginning on line 7 of page 6 with the following paragraph:

More specifically, an ATA/ATAPI Interface serves as an input **110** to receive ATA/ATAPI signals from a read unit of the mass storage device (not shown). The Disk Interface (DISK_INT) **115** receives the ATA/ATAPI signals from the ATA/ATAPI Interface **110** and transmits them the other components. The remaining chip components<u>, such as the input/output interface **140**, the RAM control circuit **144**, the global control circuit **146**, and the translate circuit (XLATE) **148**</u> provide conversion logic and are used to buffer and convert the ATA/ATAPI signals into USB 2.0 signals. The resulting USB signals are output to a USB Interface **135** through the USB 2.0 physical interface transceiver (PHY) **130**.